Abstracts

A fully integrated 40-Gbit/s clock and data recovery circuit using InP/InGaAs HBTs

H. Nosaka, E. Sano, K. Ishii, M. Ida, K. Kurishima, T. Enoki and T. Shibata. "A fully integrated 40-Gbit/s clock and data recovery circuit using InP/InGaAs HBTs." 2002 MTT-S International Microwave Symposium Digest 02.1 (2002 Vol. I [MWSYM]): 83-86 vol.1.

An integrated clock and data recovery (CDR) circuit is a key element for optical communication systems at 40 Gbit/s. We present a fully integrated 40-Gbit CDR circuit fabricated using InP/InGaAs HBTs. The circuit contains a linear-type phase detector and a full-data-rate voltage-controlled oscillator. Error-free operation and wide eye opening were obtained for 40-Gbit/s pseudorandom bit sequence (PRBS) with a length of 2/sup 23/-1. The fabricated IC dissipates 1.71 W at a supply voltage of -4.5 V.

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